Amendments to the Claims

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

testing a memory in an integrated circuit to determine a location of ~~a~~ one or more bad memory cells~~, wherein the memory is organized into one or more clusters, each of the one or more clusters having one or more memory blocks, and wherein one or more controllers operate in parallel to test at least some of the one or more memory blocks at the same time~~;

mapping out ~~an~~ one or more address locations associated with the one or more bad memory cells; ~~and~~

offsetting one or more physical address locations associated with one or more good memory cells so that logical addressing is linear and the memory appears contiguous;

determining a total memory capacity of the integrated circuit, wherein the total memory capacity does not include the one or more bad memory cells; and

binning out the total memory capacity of the integrated circuit.

2. (Currently Amended) The method of claim 1, wherein

the memory is within an integrated circuit and the testing is self-testing performed on chip by a built in self tester ~~and wherein the self tester includes the one or more controllers~~.

3. (Currently Amended) The method of claim 1, wherein

the memory is organized into one or more clusters, each of the one or more clusters having one or more memory blocks, and

mapping out of the address location associated with the bad memory cell includes mapping out a memory block having the bad memory cell.

4. (Previously Presented) The method of claim 3, wherein

offsetting one or more physical address locations associated with the one or more good memory cells is by one memory block corresponding to the size of addressable space of the memory block having the bad memory cell.

5. (Previously Presented) The method of claim 4, wherein

each of the one or more good memory cells, addressable in ascending order after the memory block having the bad memory cell, has its one or more physical address locations offset by the size of addressable space in a memory block to linearize the logical addressing.

6. (Previously Presented) The method of claim 3, wherein

there are four clusters each having four memory blocks and each memory block contains 512 kilobits of memory cells.

7. (Previously Presented) The method of claim 1, wherein

testing the memory includes

writing one or more test patterns into memory cells in the memory,

reading out data from the memory cells, and

comparing the read out data with an expected pattern of the one or more test patterns to determine a location of the bad memory cell.

8. (Original) The method of claim 7, wherein

the location of the bad memory cell is associated with an address.

9. (Currently Amended) The method of claim 1, wherein

the memory is organized into one or more clusters, each of the one or more clusters having one or more memory blocks,

one or more bad memory cells are located within one or more respective memory blocks, and

mapping out the address location includes mapping out the one or more respective memory blocks having the one or more bad memory cells.

10. (Previously Presented) The method of claim 9, wherein

offsetting the one or more physical address locations associated with the one or more good memory cells is by the one or more memory blocks associated with the number of one or more respective memory blocks having the one or more bad memory cells and the corresponding size of addressable space of the one or more memory blocks.

11. (Currently Amended) An integrated circuit comprising:

a reconfigurable memory; ~~and~~

~~a built in self tester;~~

wherein the reconfigurable memory comprises:

an array of memory cells~~, wherein the array of memory cells is organized into one or more clusters, each of the one or more clusters having one or more memory blocks~~; and

a reconfigurable memory controller to receive a logical address and generate a physical address to address the array of memory cells, the reconfigurable memory controller to map out one or more physical addresses of words having one or more bad memory cells to form a linear logical address space without addresses to words of the one or more bad memory cells,

~~wherein the built in self tester includes the one or more controllers that operate in parallel to test at least some of the one or more memory blocks at the same time~~

wherein the reconfigurable memory has a total memory capacity that does not include the one or more bad memory cells and wherein the total memory capacity is binned out during testing of the reconfigurable memory.

12. (Canceled)

13. (Previously Presented) The reconfigurable memory of claim 11, wherein the reconfigurable memory controller maps out one or more physical addresses of memory blocks having the one or more bad memory cells.

14. (Previously Presented) The reconfigurable memory of claim 13, wherein the reconfigurable memory controller includes a configuration register associated with each memory block, each configuration register including a memory block enable bit, the memory block enable bit to map out the respective memory blocks having the bad memory cells.

15. (Previously Presented) The reconfigurable memory of claim 14, wherein

each configuration register further includes a base address associated with one or more upper address bits of an address to begin the physical addressing of a respective memory block having all good memory cells.

16. (Previously Presented) The reconfigurable memory of claim 15, wherein

a value of the base address is compared with a value of the one or more upper address bits of the address to determine if each memory block having all good memory cells is selected for access.

17. (Previously Presented) The reconfigurable memory of claim 16, wherein

for a given memory block the comparison between the value of the base address and the value of the one or more upper address bits of the address results in a match and the given memory block is selected for access.

18. (Previously Presented) The reconfigurable memory of claim 11, wherein

each memory block is a self contained memory unit including an array of memory cells, an address decoder, sense amplifier array and tri-state data bus drivers.

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Previously Presented) The integrated circuit of claim 11, wherein the reconfigurable memory controller include a memory block base address.

24. (Previously Presented) The integrated circuit of claim 11, wherein the integrated circuit is an application specific integrated circuit.

25. (Original) The integrated circuit of claim 24 further comprising:
a host port.

26. (Currently Amended) The integrated circuit of claim 24 further comprising:
a memory test register; and
a built-in memory self-tester.

27. (Currently Amended) The integrated circuit of claim 24 further comprising:
a memory test register;
a built-in memory self-tester; and
a test access port.

28. (Currently Amended) The integrated circuit of claim 24 further comprising:
a host port;
a memory test register; and
a built-in memory self-tester.

29. (Canceled)

30. (Canceled)